CLAIMS

What is claimed is:

1. A circuit, comprising:

an amplifier operable to receive an input signal and a feedback signal and produce an intermediate signal; and

a variable-offset circuit operable to receive the intermediate signal and produce an output signal and the feedback signal, the output signal having a DC offset that varies corresponding to a varying parameter of the variable-offset circuit, the amplifier being operable to reduce variation of the DC offset of the output signal.

2. The circuit of claim 1, further comprising:

a correction circuit operable to receive the output signal and produce a correction signal, the correction signal being applied to the variable-offset circuit to reduce a magnitude of the DC offset of the output signal.

3. The circuit of claim 2, wherein:

the correction circuit includes,

a digital signal processor operable to measure the DC

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offset of the output signal and produce a control signal; and

a digital-to-analog converter operable to receive the control signal and produce the correction signal.

4. The circuit of claim 2, wherein:

the correction signal is a current that is applied to the variable-offset circuit.

5. The circuit of claim 2, wherein:

the correction signal is a voltage that is applied to the variable-offset circuit.

6. The circuit of claim 1, wherein:

the variable-offset circuit is a variable-gain amplifier circuit and the DC offset of the output signal varies with a gain of the variable-gain amplifier.

7. The circuit of claim 1, wherein:

the amplifier is a unity-gain buffer amplifier.

8. The circuit of claim 1, wherein:

the circuit is compliant with one or more of the Institute of Electrical and Electronics Engineers standards 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, 802.11i, 802.11n, and 802.16.

9. A circuit, comprising:

amplifying means for receiving an input signal and a feedback signal and producing an intermediate signal; and

processing means for receiving the intermediate signal and producing an output signal and the feedback signal, the output signal having a DC offset that varies corresponding to a varying parameter of the processing means, the amplifying means being operable to reduce variation of the DC offset of the output signal.

10. The circuit of claim 9, further comprising:

correcting means for receiving the output signal and producing a correction signal, the correction signal being used by the processing means to reduce a magnitude of the DC offset of the output signal.

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11. The circuit of claim 10, wherein: the correcting means includes,

digital signal processing means for measuring the DC offset of the output signal and producing a control signal; and

digital-to-analog conversion means for receiving the control signal and producing the correction signal.

12. The circuit of claim 10, wherein:

the correction signal is a current that is applied to the processing means.

13. The circuit of claim 10, wherein:

the correction signal is a voltage that is applied to the processing means.

14. The circuit of claim 9, wherein:

the processing means is a variable-gain amplifying means and the DC offset of the output signal varies with a gain of the variable-gain amplifying means.

- 15. The circuit of claim 9, wherein:

 the amplifying means is a unity-gain buffering means.
- 16. The circuit of claim 9, wherein:

the circuit is compliant with one or more of the Institute of Electrical and Electronics Engineers standards 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, 802.11i, 802.11n, and 802.16.

17. A wireless transceiver, comprising:

a receiver operable to receive a modulated carrier signal, the receiver including,

an amplifier operable to receive an input signal and a feedback signal and produce an intermediate signal; and

a variable-offset circuit operable to receive the intermediate signal and produce an output signal and the feedback signal, the output signal having a DC offset that varies corresponding to a varying parameter of the variable-offset circuit, the amplifier being operable to reduce variation of the DC offset of the output signal.

18. The wireless transceiver of claim 17, wherein:

the receiver includes a correction circuit operable to receive the output signal of the output signal and produce a correction signal, the correction signal being applied to the variable-offset circuit to reduce a magnitude of the DC offset of the output signal.

19. The wireless transceiver of claim 18, wherein: the correction circuit includes,

a digital signal processor operable to measure the DC offset of the output signal and produce a control signal; and

a digital-to-analog converter operable to receive the control signal and produce the correction signal.

20. The wireless transceiver of claim 18, wherein:

the correction signal is a current that is applied to the variable-offset circuit.

21. The wireless transceiver of claim 18, wherein:

the correction signal is a voltage that is applied to the variable-offset circuit.

22. The wireless transceiver of claim 17, wherein:

the variable-offset circuit is a variable-gain amplifier circuit and the DC offset of the output signal varies with a gain of the variable-gain amplifier.

- 23. The wireless transceiver of claim 17, wherein: the amplifier is a unity-gain buffer amplifier.
- 24. The wireless transceiver of claim 17, wherein:

 the wireless transceiver is compliant with one or more of
 the Institute of Electrical and Electronics Engineers standards
 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, 802.11i,
 802.11n, and 802.16.
- 25. A wireless transceiver, comprising: receiver means for receiving a modulated carrier signal, the receiver means including,

amplifying means for receiving an input signal and a

feedback signal and producing an intermediate signal; and

processing means for receiving the intermediate signal and producing an output signal and the feedback signal, the output signal having a DC offset that varies corresponding to a varying parameter of the processing means, the amplifying means being operable to reduce variation of the DC offset of the output signal.

26. The wireless transceiver of claim 25, wherein:

the receiver means includes correcting means for receiving the output signal and producing a correction signal, the correction signal being used by the processing means to reduce a magnitude of the DC offset of the output signal.

27. The wireless transceiver of claim 26, wherein: the correcting means includes,

digital signal processing means for measuring the DC offset of the output signal and producing a control signal;

digital-to-analog conversion means for receiving the control signal and producing the correction signal.

- 28. The wireless transceiver of claim 26, wherein:

 the correction signal is a current that is applied to the processing means.
- 29. The wireless transceiver of claim 26, wherein: the correction signal is a voltage that is applied to the processing means.
- 30. The wireless transceiver of claim 25, wherein:

 the processing means is a variable-gain amplifying means

 and the DC offset of the output signal varies with a gain of the variable-gain amplifying means.
- 31. The wireless transceiver of claim 25, wherein:
 the amplifying means is a unity-gain buffering means.
- 32. The wireless transceiver of claim 25, wherein:

 the wireless transceiver is compliant with one or more of
 the Institute of Electrical and Electronics Engineers standards
 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, 802.11i,

802.11n, and 802.16.

33. A method for reducing variation of a DC offset, the method comprising:

amplifying an input signal to produce an intermediate signal;

processing the intermediate signal to produce a feedback signal and an output signal, the output signal having a DC offset that varies corresponding to a varying parameter of circuitry used to process the intermediate signal; and

reducing variation of the DC offset of the output signal using the feedback signal.

- 34. The method of claim 33, further comprising:

 measuring the DC offset of the output signal; and
 applying a correction signal to the circuitry used to

 process the intermediate signal to reduce a magnitude of the DC
 offset of the output signal.
- 35. The method of claim 34, wherein:

 measuring the DC offset includes digitally measuring the DC

offset; and

applying a correction signal includes applying an analog correction signal produced responsive to a digital control signal, the digital control signal produced responsive to the digital measurement of the DC offset.

36. The method of claim 34, wherein:

applying a correction signal includes applying a correction current.

37. The method of claim 34, wherein:

applying a correction signal includes applying a correction voltage.

38. The method of claim 33, wherein:

processing the intermediate signal includes variably amplifying the intermediate signal; and

the DC offset of the output signal varies with a variation of the variable amplification.

39. The method of claim 33, wherein:

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amplifying the input signal includes buffering the input signal.

40. The method of claim 33, wherein:

the method is compliant with one or more of the Institute of Electrical and Electronics Engineers standards 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, 802.11i, 802.11n, and 802.16.